Optimum Design of Very High-Efficiency Microwave Power Amplifiers Based on Time-Domain Harmonic Load–Pull Measurements

Denis Barataud, Michel Campovecchio, and Jean-Michel Nebus

***Abstract*—Due to the large expansion of wireless communications, the need for high-efficiency power amplifiers has emerged. In mobile communication systems, power amplifiers are the most critical elements for the power-dissipation budget. Thus, the operating conditions of active devices have to be optimized using accurate and complementary computer-aided design (CAD) and experimental tools. This paper reports two design methods of high-efficiency power amplifiers. The first one is CAD oriented and based on the substitute generator technique using the nonlinear model of transistors. The second one is based on a specific measurement system of time-domain waveforms using a modified vector network analyzer, coupled with harmonic active load–pull techniques (three active loops). This new setup enables the measurement and optimization of time-domain waveforms at both ports of transistors driven by constant-wave test signals. These two design methodologies are applied to the optimization of an S-band 1-W class-F GaInP/GaAs heterojunction-bipolar-transistor power amplifier.**

I. Efficient CAD-Oriented Design Method of High-Efficiency Class-F Amplifiers

THE key point to optimize transistor power-added efficiency (PAE) is to appropriately control current/voltage waveforms at each port of the device. The time-domain waveform visualization gives an accurate and comprehensive insight into the actual operation mode of transistors.

The class-F operation mode of heterojunction bipolar transistors (HBTs) has already demonstrated high performances in terms of PAE at L-band [1]. Theoretically speaking, a class-F operation mode of a transistor requires: 1) a purely sinusoidal input voltage and 2) a quasi-square output voltage combined with a pulse-shaped output current. The PAE of the transistor is optimized if the overlap between the output current and output voltage is minimized (Fig. 1) so that the power dissipated by the device is minimal.

The class-F operation mode can be optimized in a straightforward manner by implementing what we call the substitute generator technique [1], [2] on any commercially available computer-aided design (CAD) tool. The principle of this CAD technique is to force the voltage waveforms at each device port by using independent voltage generators at each frequency harmonic (Fig. 2).

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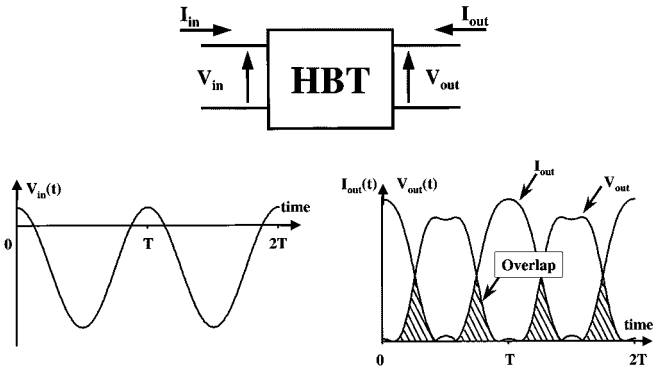

Fig. 1. Class-F operation of HBTs: intrinsic voltage/current waveforms.

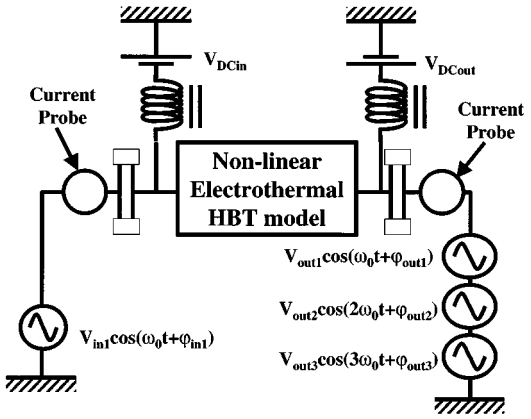

Fig. 2. Principle of the substitute generator technique.

It has to be pointed out that, in the case of HBTs, a nonlinear electrothermal model is highly necessary and can be extracted from pulsed I/V and pulsed (S) measurements [3].

For class-F optimization, a single input generator supplies the required purely sinusoidal voltage $V_{\rm in}$, while three output generators defined at f_0, $2f_0$, and $3f_0$ supply the required quasi-square voltage $V_{\rm out}$.

In this case, it has been demonstrated [4], [5] that, for a fixed output bias voltage $V_{\rm DCout}$, the optimum voltage $V_{\rm out}(t)$ to maximize the $(V_{\rm out1}/V_{\rm DCout})$ ratio is given by the expression

$$V_{\rm out}(t) = V_{\rm DCout}\left(1 - \frac{2}{\sqrt{3}}\cos(\omega_0 t) + \frac{2}{3\sqrt{3}}\cos(3\omega_0 t)\right) \tag{1}$$

where

$$V_{\rm out1} = \frac{2V_{\rm DCout}}{\sqrt{3}} \text{ and } V_{\rm out3} = \frac{2V_{\rm DCout}}{3\sqrt{3}}.$$

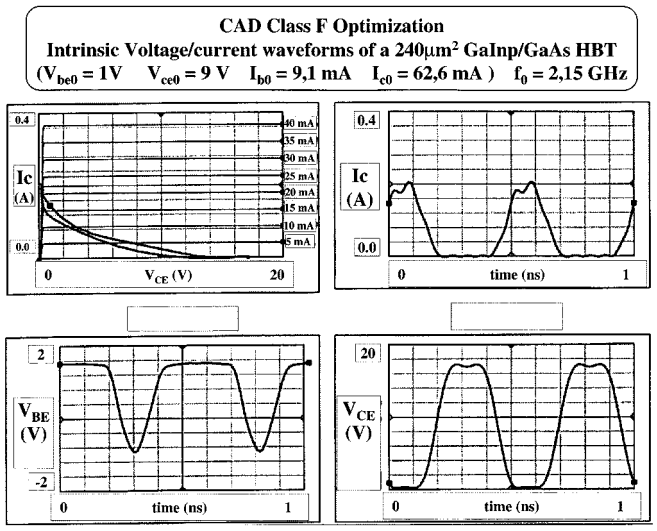

Fig. 3. Simulated waveforms and load line for a class-F operation mode of a 240-μm^2 GaInP/GaAs HBT.

TABLE I
SIMULATION RESULTS FOR A CLASS-F OPERATION MODE OF A 240-μm^2 GaInP/GaAs HBT

$P_{in}(f_0)$	$P_{out}(f_0)$	$P_{add}(f_0)$	$G_p(f_0)$	P_{diss}	P_{DC}	$PAE(f_0)$
11,2 dBm	26,6 dBm	26,4 dBm	15,3 dB	21,2 dBm	27,6 dBm	77, 1 %

$Z_{in}(f_0)$	$Z_{load}(f_0)$	$Z_{load}(2f_0)$	$Z_{load}(3f_0)$
19,7 - j 27 Ω	91,4 + j 27 Ω	0,0 - j 0,0 Ω	1,8 + j 128 Ω

These initial conditions enables us to quickly determine the optimum voltages by using few harmonic-balance analysis. Since current probes are also connected at each port of the transistor, the optimum load impedances are simultaneously determined as follows:

$$Z_{\mathrm{out}n} = -\left(\frac{\tilde{V}_{\mathrm{out}n}}{\tilde{I}_{\mathrm{out}n}}\right) \tag{2}$$

where $\tilde{V}_{\mathrm{out}n}$ and $\tilde{I}_{\mathrm{out}n}$ are the complex nth harmonic components of the output voltage and current (the constraint $\mathrm{Real}[Z_{\mathrm{out}n}] > 0$ must obviously be verified).

Fig. 3 shows the *simulated* optimum voltage and current waveforms and the associated dynamic load line at the *intrinsic* ports of a 240-μm^2 GaInP/GaAs HBT (United Monolithic Semiconductors (UMS) Foundry, Orsay, France). The optimization goal was to maximize the PAE. An optimum PAE of 77% with 15.3-dB power gain and 26.6-dBm output power have been obtained for a class-B bias point ($V_{\mathrm{CE0}} = 9$ V, $V_{\mathrm{BE0}} = 1$ V, and $I_{\mathrm{C0}} = 62.6$ mA) (Table I).

This CAD technique enables fast and systematic optimizations and can be applied to any kind of transistors as long as the nonlinear transistor model is reliable. Therefore, Section II describes an accurate and fully large-signal calibrated measurement system, which is of prime importance for validating the simulation results.

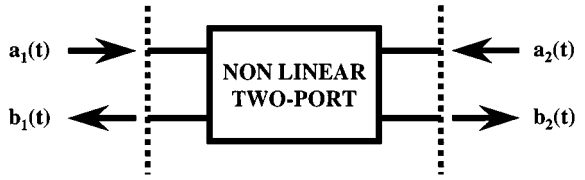

Fig. 4. Two-port nonlinear device described in the time domain.

II. EXPERIMENTAL OPTIMIZATION OF HIGH-EFFICIENCY OPERATING CLASSES OF TRANSISTORS

We have developed a new measurement system based on the use of a modified vector network analyzer (VNA). This modified VNA is coupled to a harmonic source–pull and load–pull setup. By using this measurement system, optimum operating conditions of the device-under-test (DUT) can be easily, quickly, and methodically obtained. This section reports how to experimentally control and optimize the current and voltage waveforms at each port of the DUT.

Let us consider an arbitrary two-port device described by incoming and outcoming power waves (Fig. 4).

For the extraction of time-domain waveforms, the measurements of the following signals are necessary:

$$a_i(t) = \sum_{n=0}^{N-1} a_{in}\cos(\omega_n t + \varphi_{in}) \tag{3}$$

$$b_i(t) = \sum_{n=0}^{N-1} b_{in}\cos(\omega_n t + \theta_{in}) \tag{4}$$

where i is the index of power wave and $n$is the index of frequency. Voltage/current waveforms can then be calculated with the following equations if the coefficients $(\mathbf{a}_{in}, \mathbf{b}_{in})$ and the absolute phases $(\varphi_{in}, \theta_{in})$ are accurately determined as follows:

$$v_i(t) = \sqrt{Z_0}\Big[a_i(t) + b_i(t)\Big] \tag{5}$$

$$i_i(t) = \frac{1}{\sqrt{Z_0}}\Big[a_i(t) - b_i(t)\Big] \tag{6}$$

At each frequency of interest, the power wave magnitudes $(\mathbf{a}_{in}, \mathbf{b}_{in})$ can be easily measured by using selective power meter capabilities of VNAs, but the determination of absolute phases $(\varphi_{in}, \theta_{in})$ requires a specific phase calibration of the measurement system [6], [7].

A block diagram of our measurement system with the modified VNA is shown in Fig. 5.

In the receiver operation mode, conventional VNAs can only provide sequential measurements of complex power wave ratios at each frequency of interest as follows:

$$\frac{b_{jn}}{a_{in}} e^{j(\theta_{jn} - \varphi_{in})}, \qquad \text{with } i, j = 1, 2. \tag{7}$$

Therefore, the test set of a four-channel conventional VNA has been modified by connecting a fixed reference harmonic generator to one RF channel (CH_1). The microwave source and modified VNA are synchronized with the same 10-MHz reference signal.

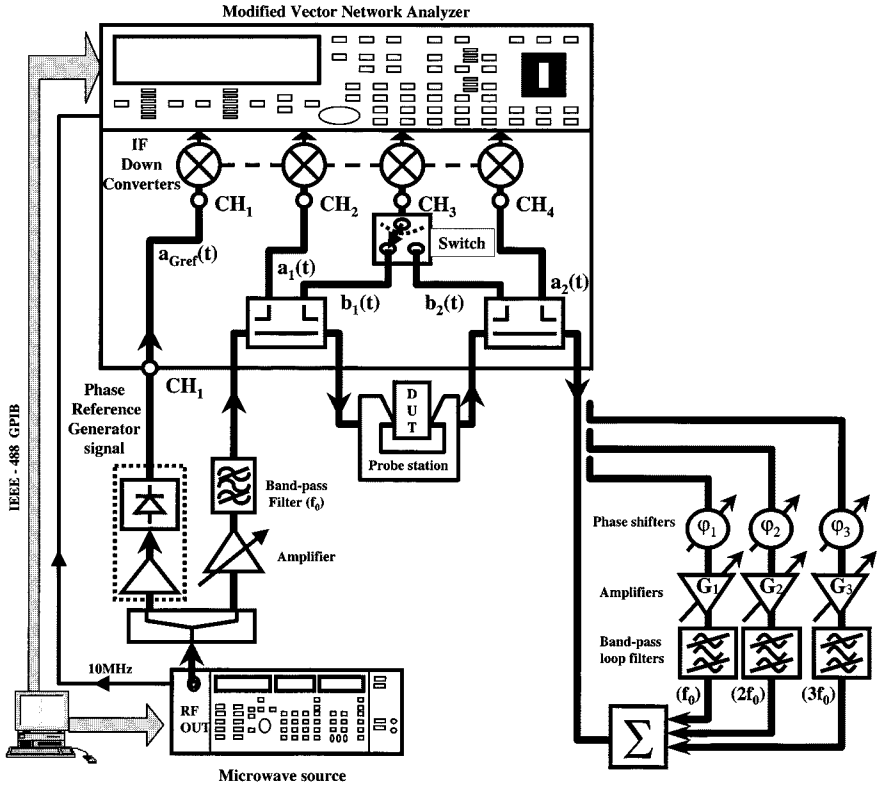

Fig. 5. Block diagram of the measurement system.

The reference harmonic generator is a step recovery diode (SRD) fed with the RF signal of the microwave source. This diode acts as a comb generator so that the output signal can be written as

$$a_{\mathrm{Gref}}(t) = \sum_{n=1}^{N} a_{\mathrm{Gref}n} \cos(n\omega_0 t + \varphi_{\mathrm{Ref}n}). \tag{8}$$

The spectrum of this reference signal must contain, at least, all the frequency components of the incoming and outcoming power waves at the nonlinear DUT ports. Therefore, to determine the absolute phases $(\varphi_{1n}, \varphi_{2n}, \theta_{1n}, \theta_{2n})$ with this modified VNA, the key idea is to measure the complex power wave ratio between b_{2n} and the fixed phase reference signal at each frequency component of interest

$$\frac{b_{2n}}{a_{\mathrm{Gref}n}} \exp\left[j(\theta_{2n} - \varphi_{\mathrm{Gref}n})\right]. \tag{9}$$

The coefficients $(a_{\mathrm{Gref}n}, \varphi_{\mathrm{Gref}n})$ are determined during the calibration procedure. Thus, as long as the signal $a_{g\mathrm{ref}}(t)$ remains constant during the calibration and the measurement procedures, the phase relationships between all harmonics of $b_2(t)$ can be determined. In the same manner, the phase relationships between harmonics of $a_1(t)$, $b_1(t)$, $a_2(t)$, and $b_2(t)$ can be determined and time-domain waveforms can be extracted.

The calibration sequence consists of the following three main steps.

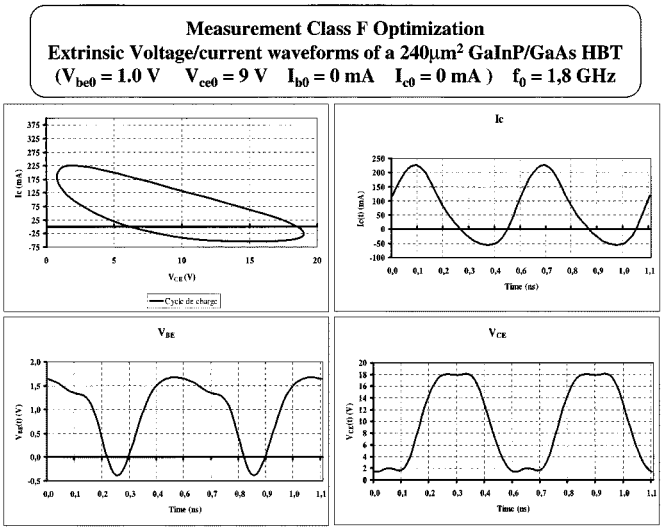

Fig. 6. Measured waveforms and load line for a class-F operation mode of a 240-μm^2 GaInP/GaAs HBT.

TABLE II
MEASUREMENT RESULTS FOR A CLASS-F OPERATION MODE OF A 240-μm^2 GaInP/GaAs HBT

$P_{in}(f_0)$	$P_{out}(f_0)$	$P_{add}(f_0)$	$G_p(f_0)$	P_{diss}	P_{DC}	$PAE(f_0)$
9,8 dBm	27,1 dBm	27,0 dBm	17,3 dB	22,2 dBm	28,2 dBm	75,5 %

$Z_{in}(f_0)$	$Z_{load}(f_0)$	$Z_{load}(2f_0)$	$Z_{load}(3f_0)$
10,8 - j 18,1 Ω	53,3 + j 42,5 Ω	0,42 - j 0,1 Ω	5393 + j 6293 Ω

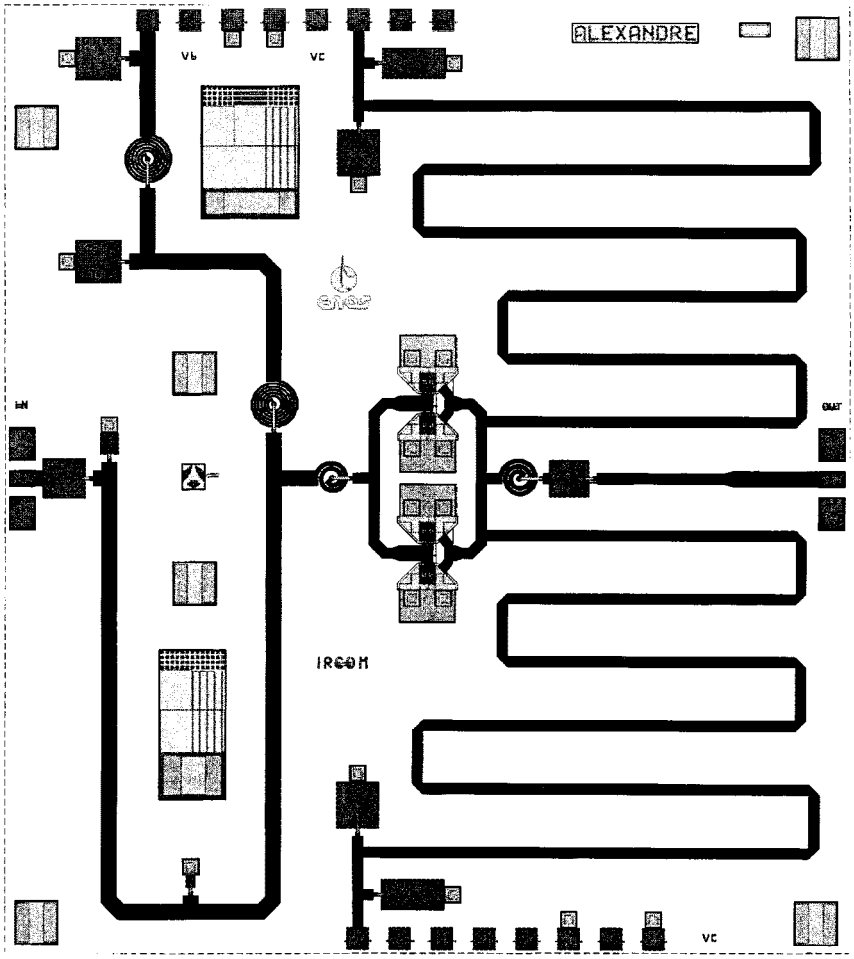

Fig. 7. Layout of the power amplifier. The chip size is 4.5 × 4 mm^2.

Step 1) Thru-reflect line (TRL) calibration for the correction of complex power wave ratios (b_{jn}/a_{in}).

Step 2) Absolute power measurements using an accurate power meter for the determination of $|a_{in}|$, $|b_{in}|$.

Step 3) Phase calibration, which is a key point. For this purpose, a second multiharmonic generator (i.e., SRD) similar to the first one (used in the reference channel of our system) is connected to the DUT reference planes. This second multiharmonic generator has been characterized using a sampling oscilloscope technique and the "nose-to-nose" procedure [8], [9].

The load–pull system based on the active loop principle is coupled to the modified VNA so that the harmonic–load impedances can be methodically tuned in order to maximize the PAE of the DUT. The key point of the whole system is that harmonic–load impedances are fully independent of transistor behaviors and input power levels. Moreover, the tuning of a loop at one frequency is independent of the loops at other frequencies. This makes the optimization process of load impedances easier and more efficient.

As an example, a 240-μm^2 GaInP/GaAs HBT (UMS Foundry) has been experimentally optimized in terms of the PAE. Fig. 6 shows the *measured* optimum voltage and current waveforms and the associated dynamic load line at the *extrinsic* ports of the transistor. An optimum PAE of 70%, with a power gain of 11.9 dB and an output power of 21.7 dBm have been obtained for a class-B bias point ($V_{\mathrm{CE0}} = 6$ V, $V_{\mathrm{BE0}} = 0.8$ V, and $I_{\mathrm{C0}} = 0$ mA) (Table II).

III. Application to the Design of an S-Band High-Efficiency HBT Power Amplifier

In collaboration with the Centre National d'Etudes Spatiales, Toulouse, France, an S-band 1-W power amplifier has been designed at the UMS foundry, in order to investigate the GaInP/GaAs HBT capabilities in terms of a PAE in class-F operation mode. The design specifications were a 10% frequency bandwidth centered on 2.15 GHz for 1-W output power and maximum PAE.

The amplifier architecture is made of one stage composed of two 240-μm^2 GaInP/GaAs HBT (UMS Foundry) biased at a class-B point ($V_{\mathrm{CE0}} = 9$ V, $V_{\mathrm{BE0}} = 1$ V). The circuit layout manufactured at the UMS foundry is shown in Fig. 7.

The PAE optimization of each transistor was simultaneously performed by using the substitute generator technique on the MDS software and the experimental technique on the previously described setup. The optimum harmonic–load impedances extracted from simulations and measurements were then compared to derive efficient and reliable goals for the amplifier design process.

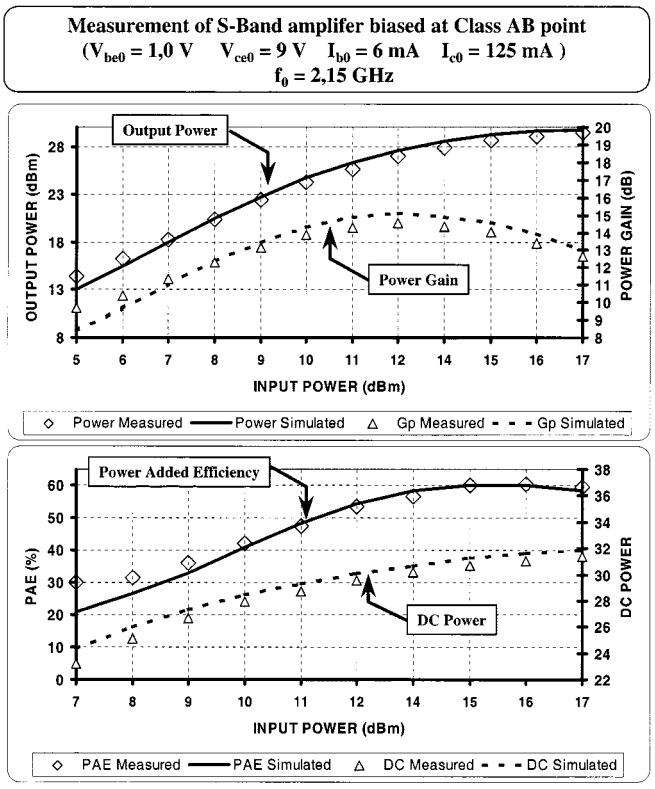

Fig. 8. Comparison between measured and simulated results of the realized MMIC optimized PAE amplifier.

The output circuit has been optimized to synthesize the optimum load impedance at the first harmonic, a short circuit at the second harmonic, and an open circuit at the third harmonic. The output matching circuit integrates two symmetrical short-circuited quarter-wave stubs to simultaneously bias each transistor and impose a short circuit at the second harmonic as close as possible to each device port.

This amplifier has been measured at the Centre National d'Etudes, at a class-AB bias point ($V_{\mathrm{CE0}} = 9$ V, $V_{\mathrm{BE0}} = 1$ V and $I_{\mathrm{C0}} = 125$ mA). The measured and simulated performances are presented in Fig. 8. The amplifier exhibited 1-W output power associated with a 60% PAE and 14-dB power gain at 2.15 GHz.

IV. Conclusion

A specific measurement setup based on the combination of an active load–pull set up with a modified VNA has been presented in this paper. By integrating a calibrated standard phase generator, this setup provides voltage and current waveform measurements at both ports of a nonlinear device. The complementary use of this setup with the CAD-oriented substitute generator technique method leads to methodic and efficient design methods of power amplifiers in terms of the PAE. It has been illustrated by a MMIC HBT power amplifier at S-band.

The measurement of high-frequency time-domain waveforms is expected to be an essential step during the modeling process of nonlinear devices. The main future investigations concern the time-domain characterization of transistors under pulsed conditions for radar applications and under complex modulated carriers.

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